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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,936	01/16/2004	Rajat Chaudhry	AUS920030974US1	8220

7590 12/05/2006

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EXAMINER	
DAY, HERNG DER	
ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 12/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,936	CHAUDHRY ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been examined and rejected.

Drawings

2. The drawings are objected to for the following reasons. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include **all** of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the Examiner, the Applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2-1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description:

(a) POWER DATA OUTPUT 660, in FIG. 6.

Specification

3. The disclosure is objected to because of the following informalities. Appropriate correction is required.

3-1. It appears that "the second logic 118", as described in lines 23-24 of page 6, should be "the second logic block 118".

3-2. As described in lines 3-5 of page 8, "An improved method is to vary the activation of the activation of the clock signals to attain a more realistic model." (Emphasis added.)

3-3. As described in lines 12-14 of page 13, "Another improved method is to vary the activation of the activation of the clock signals to attain a more realistic model and the power consumption for each LCB." (Emphasis added.)

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 14-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5-1. Claim 14 recites the limitation "The method" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

5-2. Claim 15 recites the limitation "The method" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

5-3. Claim 16 recites the limitation "The method" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 1-24 are rejected under 35 U.S.C. 101 because the inventions as disclosed in claims are directed to non-statutory subject matter.

7-1. Claims 1-24 appear to be directed merely to the manipulation of an abstract idea of approximating power consumption of a circuit with plurality of local clock buffers (LCBs) without resulting in a practical application producing a concrete, useful, and tangible result. Specifically, all the data manipulated by the claimed steps, means, or computer code would still be internal in a computer. There is no evidence any useful or tangible result has been produced in a practical application. See In *re Warmerdam,* 33 F.3d 1354, 1360 (Fed. Cir 1994).

7-2. The Examiner acknowledges that even though the claims are presently considered non-statutory they are additionally rejected below over the prior art. The Examiner assumes the Applicant will amend the claims to overcome the 101 rejections and thus make the claims statutory.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Radjassamy, U.S. Patent Application Publication No. 2004/0186703 A1 Published September 23, 2004, and filed March 20, 2003, in view of Lim et al., U.S. Patent 5,481,209 issued January 2, 1996.

9-1. Regarding claim 1, Radjassamy discloses a method for approximating power consumption of a circuit with plurality of local clock buffers (LCBs), comprising:

inputting a Hardware Descriptive Language (HDL) simulator data of the circuit (The HDL language environment provides a design, simulation, and synthesis platform, paragraph [0015]);

inputting net capacitance data of the circuit (as shown in FIG. 4, capacitance are associated with various power consumption components as capacitors);

inputting energy model data (power consumption equation P_{EST}, for power consumption component models shown in FIG. 5A-5F); and

generating power consumption data from the HDL simulator data, the capacitance data, and the energy model data (the power consumption of the entire sub-block may be estimated, paragraph [0086]).

Radjassamy fails to expressly disclose wherein the energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs.

Lim et al. disclose an apparatus and method for improved clock distribution and control in an integrated circuit having the ability to selectively inhibit clock signals at the local buffer 46. Using inhibit 52 to inhibit the clock at selected locations of the integrated circuit 10 allows for reduction of power dissipation (column 4, lines 62-67). Other features include locally buffered clock signals and multiple clock enables (column 3, lines 33-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Radjassamy to incorporate the teachings of Lim et al. to obtain the invention as specified in claim 1 because inhibiting locally buffered clock signals at selected locations results in reduced estimation of power dissipation as suggested by Lim et al.

9-2. Regarding claim 2, Radjassamy further discloses wherein each LCB of the plurality of LCBs is at least configured to consume the same amount of power (for example, I_i represents the current of clock type i, paragraph [0044]; same current for same clock type).

9-3. Regarding claim 3, Radjassamy further discloses wherein the energy model data further comprises extrapolating energy data by increasing or decreasing numbers of active input signals to the circuit (for example, activity factors, paragraph [0067]).

9-4. Regarding claim 4, Radjassamy further discloses wherein the method further comprises inputting template data, wherein the template data is at least configured to contain relative power consumption data for each LCB of the plurality of LCBs (as shown in FIG. 4 and FIG. 5A-5F, each of the various power consumption components may have its own clock input).

9-5. Regarding claim 5, Radjassamy further discloses wherein the relative power consumption data of each LCB of the plurality of LCBs are at least configured to be the same or different (for example, I_i represents the current of clock type i, paragraph [0044]; same current for same clock type).

9-6. Regarding claim 6, Radjassamy further discloses wherein each LCB of the plurality of LCBs is at least configured to consume the same amount of power (for example, I_i represents the current of clock type i, paragraph [0044]; same current for same clock type).

9-7. Regarding claim 7, Radjassamy further discloses wherein the energy model data further comprises extrapolating energy data by increasing or decreasing numbers of active input signals to the circuit (for example, activity factors, paragraph [0067]).

9-8. Regarding claim 8, Radjassamy further discloses wherein the generating power consumption data is at least configured to utilize the template data (the power consumption of the entire sub-block may be estimated by aggregating the power consumption estimates of its constituent power consuming components, paragraph [0086]).

9-9. Regarding claims 9-16, these apparatus claims include equivalent method limitations as in claims 1-8 and are unpatentable using the same analysis of claims 1-8.

9-10. Regarding claims 17-24, these program product claims include equivalent method limitations as in claims 1-8 and are unpatentable using the same analysis of claims 1-8.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Reference to Minami et al., U.S. Patent 6,272,667 B1 issued August 7, 2001, is cited as disclosing a method for clock gated logic circuits to reduce electric power consumption.

Reference to Khouja et al., U.S. Patent 6,345,379 B1 issued February 5, 2002, is cited as disclosing a method for estimating internal power consumption of an electronic circuit.

Reference to Saxena et al., U.S. Patent 6,810,482 B1 issued October 26, 2004, and filed January 26, 2001, is cited as disclosing power estimation through the use of an energy macro table.

Reference to McGuffin et al., U.S. Patent 7,000,204 B2 issued February 14, 2006, and filed September 2, 2003, is cited as disclosing power estimation based on power characterizations.

Reference to Shen et al., U.S. Patent 7,051,300 B1 issued May 23, 2006, and filed September 4, 2003, is cited as disclosing architectural power estimation.

Reference to Keller et al., U.S. Patent 7,086,019 B2 issued August 1, 2006, and filed August 25, 2003, is cited as disclosing a method for determining activity factors of a circuit design.

Reference to Ravi et al., U.S. Patent Application Publication 2004/0019859 A1 published January 29, 2004, and filed July 29, 2002, is cited as disclosing a method for efficient RTL power estimation.

Reference to Chen, U.S. Patent Application Publication 2004/0236560 A1 published November 25, 2004, and filed May 23, 2003, is cited as disclosing power estimation using functional verification.

Reference to Neely et al., "CPAM: A Common Power Analysis Methodology for High-Performance VLSI Design", IEEE Conference on Electrical Performance of Electronic Packaging, October 2000, pages 303-306, is cited as disclosing a formula to calculate the total chip power.

Reference to Brooks et al., "Power-Aware Microarchitecture: Design and Modeling Challenges for Next-Generation Microprocessors", IEEE Micro, Volume 20, Issue 6, 2000, pages 26-44, is cited as disclosing energy models.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
October 27, 2006 H.D.

FRED FERRIS
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100